WHAT IS CLAIMED IS:

1. An integrated circuit wafer comprising:

a wafer comprising a substrate comprising a wafer material, said substrate having first and second surfaces, said first surface having a circuit layer comprising integrated circuit elements constructed thereon;

a plurality of vias extending a first distance from said first surface of said substrate into said substrate, said vias comprising a stop layer comprising a stop material that is more resistant to chemical/mechanical polishing (CMP) than said wafer material, said vias being filled with an electrically conducting material forming a conducting plug extending from said top surface of said substrate into said substrate, said plug having a top portion proximate to said first surface and bottom portion, said top portion having a cross-sectional area that is greater than that of said bottom portion of said plug, wherein said top portion of said plug comprises a recessed region sized to receive an end of a bottom portion of one of said plugs from a second one of said integrated circuit wafers.

2. The integrated circuit wafer of Claim 1 wherein said recessed region comprises a via in an insulating layer on said first surface of said substrate.

3. The integrated circuit wafer of Claim 1 wherein said recessed region comprises a depression in said plug.

4. The integrated circuit wafer of Claim 1 wherein said stop material comprises a material chosen from the group consisting of Ta, TaN, W, WN, $Ta_xSi_yN_z$, W_2, and Si_yN_z, and wherein said wafer material comprises silicon.

5. The integrated circuit wafer of Claim 1 wherein said vias are lined with a layer of an electrically insulating material.

6. The integrated circuit wafer of Claim 5 wherein said electrically insulating material comprises SiO_2.

7. The integrated circuit wafer of Claim 5 wherein said vias are filled with an electrically conducting material.

8. The integrated circuit wafer of Claim 7 wherein said electrically conducting material comprises an element chosen from the group consisting of copper, tungsten, platinum, and titanium.

9. The integrated circuit wafer of Claim 1 further comprising:

a dielectric layer having top and bottom surfaces, said dielectric layer covering said circuit layer such that said bottom surface is in contact with said integrated circuit layer; and

a plurality of electrical conductors buried in said dielectric layer and making electrical connections to said integrated circuit elements.

10. The integrated circuit wafer of Claim 9 wherein at least one of said vias extends through said dielectric layer and wherein said one of said vias is filled with an electrically conducting material, said via terminating in an electrically conducting pad on said top surface of said dielectric layer.

11. The integrated circuit wafer of Claim 10 wherein said electrically conducting pad extends above said top surface of said dielectric layer.

12. The integrated circuit wafer of Claim 10 wherein one of said electrical conductors is connected electrically to said one of said vias.

13. A method for adding a second circuit layer to a first wafer comprising a first

circuit layer, said method comprising the steps of:

providing a plurality of bonding pads on a first surface of said first wafer;

providing a second wafer comprising a substrate of a wafer material and said second circuit layer, said second circuit layer being fabricated on a first surface of said substrate and being covered by a layer of dielectric material, said wafer further comprising a plurality of vias extending a predetermined distance from said first surface of said substrate into said substrate, said vias including a layer of stop material, said stop material being more resistant to CMP than said wafer material;

providing a plurality of bonding pads on said second wafer, there being a one to one correspondence between said bonding pads on said first and second wafers;

positioning said first and second wafers such that said bonding pads on said first wafer are brought in contact with said bonding pads on said second wafer;

causing said corresponding bonding pads to bond to one another; and

thinning said second wafer by removing a portion of said second wafer by CMP of the surface of said second wafer that is not bonded to said first wafer, said stop layer in said vias determining the amount of material that is removed, wherein said vias are filled with a conducting material thereby forming a plug extending from said surface of said second wafer having said bonding pads to said stop layer and wherein said step of thinning said second wafer leaves a portion of said plugs elevated above said surface of said second wafer remaining after removing said portion of said second wafer.

14. The method of Claim 13, wherein said stop material comprises a material chosen from the group consisting of Ta, TaN, W, WN and wherein said wafer material comprises silicon.

15. The method of Claim 13 further comprising the steps of:

providing a third wafer having bonding pads on one surface thereof, said bonding pads being positioned to engage said portions of said plugs that extend above said surface of said second wafer;

positioning said third wafer relative to said second wafer such that said bonding pads on said third wafer will contact said portions of said plugs that extend over said surface on said second wafer when said second and third layers are brought together; and

bonding a third wafer to said portions of said plugs that extend above said surface of said second wafer.

16. The method of Claim 15 wherein said bonding pads on said surface of said third wafer comprise a depressed region sized to engage said elevated portions of said plugs on said surface of said second wafer.

17. The method of Claim 15 wherein said step of positioning said third wafer comprises using said positions of said plugs in said second wafer to determine the relative position of said second and third wafers.